

Title: From asymptotic PRAM speedups to easy-to-obtain concrete XMT ones

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Abstract:

Considering a horizon where the transistor count of a chip would be in the billions, our SPAA 1998 explicit multi-threading (XMT) platform paper envisioned a framework extending from PRAM-style algorithms to architecture. Through steady and methodical progress, 2011 marks a point where prototyping meets many more of the 1998 original objectives: we can now show strong speedups on some of the most advanced PRAM algorithms, often far exceeding speedups obtained for commercial platforms. XMT speedups are also much easier to derive, and the thermal envelope of XMT appears to not fall behind commercial processors.

The main industry players designated multi-core machines coupled with parallel programming as the only remaining avenue for maintaining the celebrated Moore's Law on track for general-purpose computing. Time permitting, I will review a variety of recent data points suggesting significant gaps between stated industry objectives and what has been delivered to date.

Homepage of the XMT project: www.umiacs.umd.edu/users/vishkin/XMT/